

CUSTOMER NO.: 24498
Serial No. 10/583,822
Office Action dated: 10/15/08
Response dated: 02/12/09

PATENT
PD030129

Remarks/Arguments

Claims 17-26 are pending in the Application. Claim 17-26 are rejected by Examiner. Claims 1, 8, 14, and 24 are amended by Applicant. Claims 21 and 25 are cancelled in this amendment without disclaimer or prejudice. The Figures have been objected to. Claim 17 has also been objected to.

Amendments to the Claims

Claim 17 has been amended to clearly recite a circuit, in which a common control signal line is connected to the control electrodes of the current control means of a multiplicity of elements in such a way that a corresponding multiplicity of current mirror circuits connected in parallel are formed. This amendment is fully supported at least by Figure 12 and the description thereof.

Claim 18 has been amended to remove matter already present in claim 17.

Claim 20 has been amended to achieve consistency of terms used in preceding claims.

Claim 21 has been cancelled.

Claim 23 has been amended to better reflect the inventive driving method as described with reference to the description of Figures 5 and 12.

Claim 25 has been cancelled.

No new matter has been added.

Objection to the Figures

The Figures have been objected to under 37 CFR 1.83(a) for failing to show every feature of the invention specified in the claims. Specifically, the Examiner asserts that the fourth switching means from claims 21 and 25 is not shown.

Claims 21 and 25 have been cancelled in this response removing recitation of a fourth switching means from the claims. As such, Applicant respectfully requests that the Examiner withdraw the objection to the Figures.

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Objections to the Claims

Claim 17 has been objected to for ending in a comma rather than a period. Claim 17 has been amended as suggested by the Examiner so that it now ends in a period. As such, Applicant respectfully requests that the Examiner withdraw the objection to Claim 17.

Claim Rejections Pursuant to 35 U.S.C. §103

Claims 17-20 and 22-26

Claims 17-20 and 22-26 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,917,350 to Pae et al. ("Pae") in view of U.S. Patent No. 7,138,967 to Kimura ("Kimura"). Applicant respectfully traverses the rejection.

Claim 25 has been cancelled in this response rendering the rejection to the claim 25 moot.

One aspect of the present application set forth in the claims is selectively coupling one half of a current mirror to one or a group of pixel cells, each one comprising only the other half of the current mirror circuit. Thus, when the two serially connected switches of a pixel cell of the inventive circuit are closed, the half-circuit of a current mirror of the respective pixel cell is operatively connected to the other half-circuit external to the pixel cell. This is a concept that is not disclosed, taught or suggested in either Pae or Kimura.

As discussed in the present application, both OLED and TFT transistors suffer from variations in their electrical parameters due to manufacturing process variations. In OLED, the luminance is substantially linearly dependent from the current, while the forward voltage for a certain current may vary substantially. The same applies to the gate-source threshold voltage of TFT transistors.

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Driving the current control means of active matrix OLED displays can be done in essentially two different ways: Using a control current, or using a control voltage.

Using a control *voltage* advantageously allows for a low output impedance of the driver, which in turn allows for quickly charging parasitic capacitances during the control period. However, the relation between the voltage and the current, which eventually translates into the desired light output, is far less determined than is desirable for achieving acceptable uniformity of light output. This needs to be taken into account when designing the display, and is usually done by providing a closed feedback loop for driving. That is, when the control voltage of the pixel is set, the output current is measured and, if necessary, corrected. This is exactly what is done in Pae. During setting the control voltage in the capacitor of the pixel cell, the OLED is disconnected from the current control means and the current is fed to a comparator that compares the actual output current with a desired reference value. A ramp voltage is applied to the current control means until the comparator toggles and signals that the desired value has been reached. Only then the OLED is switched on and the comparator is disconnected from the current control means (signals SEL1 and /SEL being logically opposite signals).

When a control *current* is used for controlling an active matrix OLED display a current mirror circuit copies a control current into the current control means of the respective pixel cells. The current control means may or may not be provided with a signal holding means, usually a capacitance that maintains the gate-source voltage. However, since the OLED and the TFT transistors have a well defined current characteristic, when compared to the much less defined voltage characteristic, no closed feedback loop is required. Rather, when the control current is known, so is the current actually flowing through the current control means of the respective pixel cell.

Kimura discloses using two serially connected switches connecting the control line and the current control means as well as using current control for programming the individual pixel cells. However, Kimura teaches providing an individual current mirror for each of the pixel cells, which adds to the complexity of the display circuit.

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The control method of Kimura includes setting a constant current in the current supply and modulating the constant current in a separate switch circuit by turning the current on or off. The constant current is refreshed only at longer intervals that need not necessarily be synchronised with the display refresh rate.

The present application involves selectively coupling one half of a current mirror to one or a group of pixel cells, each one comprising only the other half of the current mirror circuit. Thus, when the two serially connected switches of a pixel cell of the inventive circuit are closed, the half-circuit of a current mirror of the respective pixel cell is operatively connected to the other half-circuit external to the pixel cell. The reference current ramp flowing through the external half of the so-established current mirror is identically copied into each one of the connected pixel cells that has both switches closed. This in turn only requires determining, or measuring, the reference current in a single point in the circuit, while still being able to know the current actually flowing in each one of the connected pixel cells. When the actual reference current reaches a level that equals the desired level for one of the pixel cells that is operatively connected in a current mirror circuit it is sufficient to open one of the two switches for that particular pixel cell. When a signal holding means is connected, this level will be maintained until it is reprogrammed. Otherwise the current flow in the disconnected pixel cell will decay and eventually cease.

The present application advantageously allows for programming a multiplicity of pixel cells *simultaneously* using only one single current ramp signal, and one single current measuring means provided in the driving circuit. This is an advantage because using current mirrors, or current sources in general, involves comparatively large impedances at the source side of the circuit, which may lead to slow programming due to resistances and parasitic capacitances in the circuit. If individual pixel cells were to be programmed one after the other, the slow programming may limit the refresh rate of the display. Slow programming in the current programming mode may be compensated for by providing a number of parallel circuits for programming cells in parallel, but this would undesirably increase the circuit complexity.

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Applying the teaching of Kimura to Pae by providing two serially connected switches (P1 plus one further transistor) in the connection between the data line and the control electrode of the current control means (gate of P0) would not make sense to the person of ordinary skill in the art, because Pae teaches voltage control of the pixel cells and needs a separate closed control loop for each of the pixel cells to properly operate. Individual closed loop control, however, by its nature excludes programming multiple parallel circuits using only one reference driving signal. The signal "ramp" in Pae that is supplied to the control electrode of the current control means is maintained at a certain level once the comparator determines that the actual current of the pixel cell is equal to the reference signal "Vref" supplied to the deviation compensator 20 of figure 3. Because the control loop is closed, the "ramp" signal applied to the data line no longer increases, even if the "Vramp" signal of the S&H circuit does. Consequently, any other pixel cell simultaneously connected to the same data line would receive a signal that no longer increases, and would never reach a final value that is higher than the lowest value of the pixel cells connected in parallel.

The only point in Pae at which a common ramp signal can be used is Vramp at the input of the S&H circuit 23 in figure 3. However, this is not the same control signal as the ramp signal in the inventive circuit and method. It is applied at a totally different point of the circuit, and serves a different purpose.

Applicant is unable to identify a reason why and how the person of ordinary skill in the art would modify the circuit of Pae to achieve the claimed invention. In fact, as shown further above, the simple replacement of the single switch in Pae with the two serially coupled switches in Kimura does not lead to the inventive circuit. As such, the improvement presented in the present application is more than the predictable use of prior art elements according to their established functions, and the invention is not obvious in over Pae in view of Kimura.

In view of the discussion above, the display of claims 17-20 and 22 is not obvious and is patentable over Pae in view of Kimura. As such, Applicant respectfully

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request that the Examiner withdraw the rejection to claims 17- 20 and 22 and pass the claims to issue.

Likewise, the method recited in claims 23-26 is also not obvious over the two references, since Pae teaches a closed loop control for a voltage drive control of the display, while Kimura teaches a control of the display using a constant current that is set once and then modulated. These two control methods are completely different from each other and cannot be mixed with each other in order to obtain the method presented in the present application.

In view of the discussion above, the circuit of claims 23-24 and 26 is not obvious and is patentable over Pae in view of Kimura. As such, Applicant respectfully requests that the Examiner withdraw of the rejection to claims 23-24 and 26 and pass the claims to issue.

Claim 21

Claim 21 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Patent No. 6,917,350 to Pae et al. ("Pae") in view of U.S Patent No. 7,138,967 to Kimura ("Kimura") and further in view of U.S. Patent No. 6,246,180 to Nishigaki ("Nishigaki").

Claim 21 has been cancelled in this response rendering the rejection to the claim moot.

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Conclusion

Applicant respectfully submits that the amended pending claims patentably define over the cited art and respectfully requests reconsideration and withdrawal of the 35 U.S.C. §103 rejection of the pending claims. Renewed reconsideration for a Notice of Allowance is respectfully requested.

Please charge the \$130.00 fee for the One-Month Extension of Time, and any other fees that may be due to Deposit Account No. 07-0832 therefore.

Respectfully submitted,

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